REMARKS

Claims 2-4 and 26-30 that have been acted upon remain pending. New claims 31-35 are being added by this Amendment.

Claim Rejections Under 35 U.S.C. §102

Claims 2-4, 28 and 29 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Application Publication No. 2002/0099904 A1 to Conley ("Conley"). This rejection is respectfully traversed.

Each of these claims specifies that a block of memory cells is selected for storage of received data on the basis of the number of units of that data which have sequential logical addresses. The application of the Conley reference in the final Office Action appears to be equating logical addresses of data received from a host with the physical addresses of the memory at which the received data are stored, which, if this is being correctly understood, is believed to be incorrect.

In paragraph 0062 of Conley, which is relied upon by the Office Action, the selection of the block of memory cells into which received data are to be written is based upon the amount of erased data storage capacity of various blocks. In the "Response to Arguments" section of the Office Action (paragraph 5, 2nd paragraph on page 6), this aspect of Conley is correctly described. But what is respectfully submitted to be incorrect is equating this with selecting a physical block in which received data are to be written based upon the number of sequential logical addresses of the received data, as is claimed. As described in paragraph 0010 of the Background of the present application and illustrated in the illustrative example of Figure 18, the host assigns logical addresses to the data and then send the data to the memory system with these logical addresses. The memory system then translates the received logical addresses into available physical addresses of the memory and stores the received data at those physical addresses.

The claimed memory system operation decides upon a physical block in which to store data received with a host command on the basis of the number of sequential logical addresses of the received data. If that number is greater than a given proportion (or fraction) of the storage

capacity of a memory cell block, then the data are stored in one block, but if equal to or in excess of that given proportion (or fraction), then the data are stored in another memory cell block. This is independent of whatever constraints may exist as to the available physical storage capacity of the blocks. But the use of the available physical storage capacity of the blocks to decide where to write received data is the aspect of Conley that appears to be relied upon by the Office Action to reject the claims. Conley's choice of a memory cell block based on its physical capability to store received data is respectfully submitted to be much different from and not to anticipate the claimed use of a number of sequential logical addresses of the received data to make the block choice.

The reason for selecting a physical block based on the number of sequential logical addresses of the received data is to reduce consuming overhead operations of the memory that are necessary to handle repeated re-writes of small amounts of data, particularly single sector rewrites. When an amount of data with sequential logical addresses being written is small when compared to the storage capacity of a memory cell block, prior art techniques typically require that such data first be written into a fully erased block and then consolidated with other data in another erased block in order to make good use of the storage capacity of the memory. The techniques claimed in the present application reduce the amount of such data consolidation by writing small amounts of data (less than a given proportion or fraction of a block) into a common block. A number of such small amounts of data may therefore be written into a common designated block before consolidation of data becomes necessary, rather than the prior art techniques that use entire erased blocks to receive such data and then thereafter require the frequent consolidation of data in order to reclaim the large amounts of erased memory capacity remaining in these blocks. Data consolidation includes copying some data from one block to another, which is a time consuming process that can affect the overall performance of the memory system to do other things. So a reduction of the frequency of data consolidation operations significantly benefits operation of the memory system.

Claim Rejections Under 35 U.S.C. §103

Claims 26, 27 and 30 have been rejected under 35 U.S.C. §103(a) as being unpatentable over Conley as applied to claims 1 (sic: claim 2?) and 28, and further in view of U.S. Patent

Application Publication No. 2002/0034105 A1 to Kulkarni et al. ("Kulkarni"). This rejection is also respectfully traversed, for the reasons given above for the parent claims of this group of dependent claims and because Kulkarni describes a completely different process than that being claimed.

Kulkarni describes a way of writing large files to flash memory. As described in paragraphs 0013 and 0014 specifically identified in the Office Action, an amount of received data are accumulated and temporarily stored in volatile memory (RAM) until at least fifty percent of the capacity of a flash memory block is so stored, at which time the data are written from the RAM to a block of flash memory. This different process, with a different purpose, than that being claimed is respectfully submitted not to have rendered obvious the use of the claimed 25-75 proportion (or fraction) of the capacity of a memory cell block to make the decision of which memory cell block the data will be written to. Kulkarni uses this percentage breakpoint to decide when to write accumulating data into flash memory, not to decide which of at least two blocks data will be written, as claimed.

New Claims

New claims 31-35 also contain the limitations discussed above with respect to claims 2 and 28 that distinguish the cited Conley reference. In addition, these claims recite the making of a choice of which physical block received data are to be stored on the basis of the block storage capacity. This is the feature of Conley that the Office Action contends anticipates making the claimed choice of a physical memory block on the basis of the number of sequential logical addresses. The new claims then also additionally include this feature of selecting a physical block for writing data on the basis of the number of sequential logical addresses of the received data. The characteristic of the memory system to translate between logical addresses of received data and physical addresses of where that data are stored is also included in the preamble to clearly distinguish the two types of addresses.

Conclusion

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters

that need to be resolved, a telephone call to the undersigned at 415-318-1163 would be appreciated.

FILED VIA EFS

Respectfully submitted,

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